

Noise performance of submicron HEMT channels under low power consumption operation

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We have investigated the noise performance of HEMT devices for low noise operation with the aim of developing a noise model valid for low power biasing. Analytical expressions useful for CAD models have been derived for the calculation of the Pospieszalski gate and drain temperatures, and have been verified from near pinchoff conditions up to usual bias voltages. An overshoot in the drain temperature as a function of the drain voltage has been observed at low drain currents in deep submicron gate length devices.

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